Peer/Instructor Review Meeting #1

Group:
sdmay21-10

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Project Goal

Detect breach in Control-Flow Integrity using dynamic programming on an FPGA board

- Create race logic in Java and C
- Complete testing for both
- Hardware integration

Technical Challenge - Race Logic

- Creating Race Logic algorithm
  - Started in Java and moving down to lower-level language
  - I.E., From Java to C to the FPGA board.
- Test the Race Logic algorithm
  - Junit
  - Cunit
- Determining appropriate output for the algorithm

Race Logic

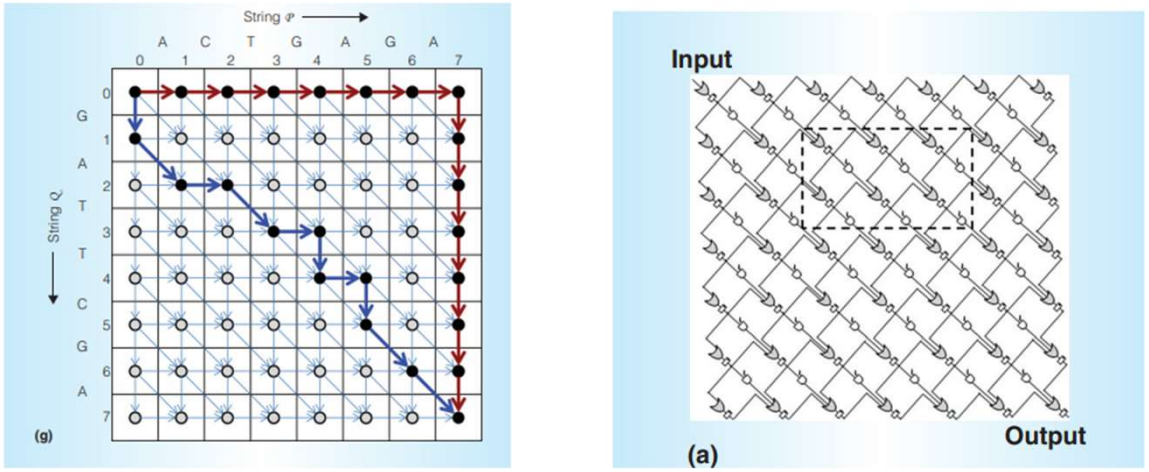

Figure 3.1: Race Logic

A. Madhavan, T. Sherwood and D. Strukov, "Race Logic: Abusing Hardware Race Conditions to Perform Useful Computation," in *IEEE Micro*, vol. 35, no. 3, pp. 48-57, May-June 2015, doi: 10.1109/MM.2015.43.

Basic Proposed FPGA Design

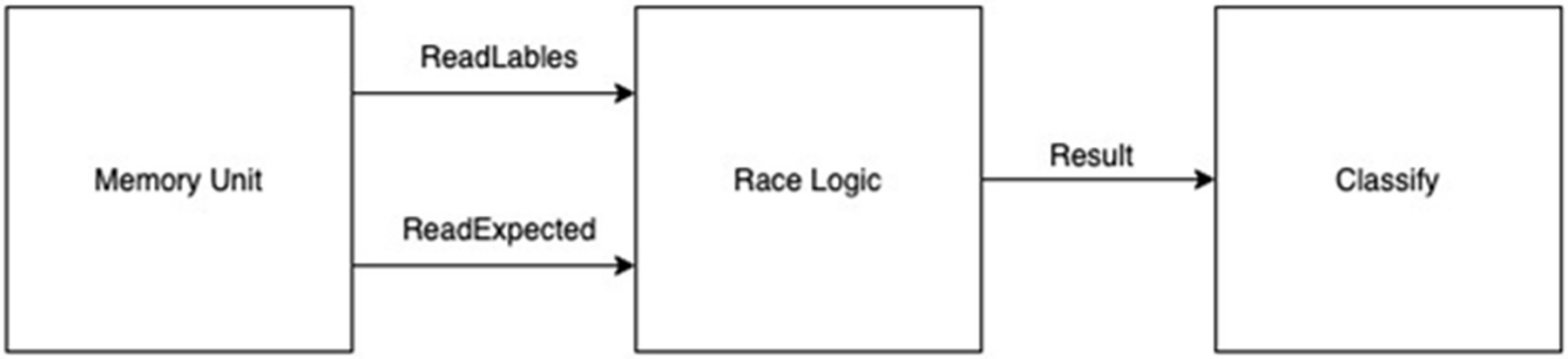

Figure 3.2: FPGA Design schematic

Technical Challenge - FPGA

- Converting our Java solution to VHDL
  - FSM (Finite State Machine)
- 8-bit inputs
- Debugging
  - Modelsim
- Translating from Modelsim to actual FPGA board
  - Altera Quartus Prime

Technical Challenge -LLVM

LLVM: compiler and toolchain

Convert source code to Intermediate Representation (IR)

- Portable, high-level assembly language

Passes: transformations and optimizations to the program

- Our pass will insert some label at each basic block in the program