# EE/CprE/SE 492 - sdmay21-10
# Dynamic Programming Based FPGA Hosted Control-Flow Integrity (CFI)
# Report 2

*February 8th - February 22nd*
*Client: Akhilesh Tyagi*
*Faculty Advisors: Zelong Li, Ananda Biswas*

## Team Members

Gregory Wendt - Meeting Scribe
Cole Schumacher - Meeting Facilitator
Nickolas Mitchell - Chief Engineer (FPGA)
Sam Henley - Chief Engineer (Software)
Maxwell Wangler - Test Engineer
Tristan Duyvejonck - Report Manager

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## Past Weeks Accomplishments

Over the past two weeks, our team continued testing our software solution and began development of our FPGA solution. Maxwell has created the logic to input 8-bit strings which hope to test within the next reporting period. Nick has created a test VHDL program in Modelsim to explore the language and test environment. Nick hopes to build off this throughout the next reporting period to develop a finite state machine and make progress on our final FPGA solution. Lastly, Sam continued development and research of LLVM passes while Greg updated our design document and corrected some outdated code on our Github.

## Pending Issues

- Work towards a better understanding of LLVM compilers
- Create FSM using Java code for FPGA solution
- Research translating Modelsim VHDL project to FPGA board
- Test 8-bit string inputs

## Individual contributions

| NAME | Individual Contributions (Quick list of contributions. This should be short.) | Hours this week | HOURS cumulative |
|---|---|---|---|
| Gregory Wendt | Added runtime detail to design document, fixed code that was in the wrong Github, and added comments | 2 | 8 |

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|---|---|---|---|
| Cole Schumacher | Was not able to contribute outside of meetings | 0 | 1 |
| Nickolas Mitchell | Started working with VHDL and Modelsim, begun development of FPGA solution | 5.5 | 16.5 |
| Sam Henley | Start looking into developing an LLVM passes | 2 | 5 |
| Maxwell Wangler | Created logic to take in tags and add them to the correct array. | 3 | 7 |
| Tristan Duyvejonck | Was not able to contribute outside of meetings | 0 | 1 |

## Plans for the Upcoming Report

- Gregory
    - Work with Max to test 8bit instructions
    - Potentially explore documentation to see what else can be better explained
- Cole
    - Help Nick with FSM and VHDL code
- Nickolas
    - Create FSM for using our Java code
    - Continue working with VHDL and Modelsim
        - Obtain better understanding of these two things
        - Demonstrate workable code necessary for our project
- Sam
    - Continue testing and developing LLVM passes
- Maxwell
    - Test 8bit instructions
- Tristan
    - Help Sam with LLVM passes