EE/CprE/SE 492 - sdmay21-10
Dynamic Programming Based FPGA Hosted Control-Flow Integrity (CFI)
Report 1

January 25th - February 8th
Client: Akhilesh Tyagi
Faculty Advisors: Zelong Li, Ananda Biswas

Team Members

Gregory Wendt - Meeting Scribe
Cole Schumacher - Meeting Facilitator
Nickolas Mitchell - Chief Engineer (FPGA)
Saml Henley - Chief Engineer (Software)
Maxwell Wangler - Test Engineer
Tristan Duyvejonck - Report Manager

Past Weeks Accomplishments

Please note, we have included in the work and estimated hours completed within this report.

For our first two weeks back, we reorganized as a team and met with the client about semester plans. The changes made to the race logic were cleared to be a part of the main code. Greg found a bug in the race logic that excluded the last variable and fixed it. Our team also completed some work over winter break such as race logic testing and design document modification. During the break, Nick completed research and a basic diagram of the FPGA solution while Maxwell developed more unit tests to ensure our racelogic algorithm works as expected.

Pending Issues

- Work towards a better understanding of LLVM compilers
- Begin development of FPGA solution
- Test 8-bit string inputs

Individual contributions

NAME	Individual Contributions (Quick list of contributions. This should be short.)	Hours this week	HOURS cumulative
Gregory Wendt	Modification and testing of Java race logic. Helped on documentation.	6	6
Cole Schumacher	Research into different FPGA options and implementation methods	1	1
Nickolas Mitchell	Researched FPGA solution, scheduled meetings, worked on design document, created rough FPGA design diagram	11	11
Sam Henley	Research LLVM transform passes	3	3
Maxwell Wangler	Added more coverage to the test suite. Helped work on documentation.	4	4
Tristan Duyvejonck	Presentation Preparation	1	1

Plans for the Upcoming Report

- Gregory
  - Explain race logic better in documentation
  - Work with Max to test 8bit instructions
  - Potentially explore documentation to see what else can be better explained
- Cole
  - Begin presentation for PIRM 1
  - Schedule team and client meetings
  - Continue research into effective and efficient ways to utilize our FPGA board.
- Nickolas
  - Begin implementation of FPGA solution
    - Work towards translating our Java racelogic algorithm to an FPGA board
  - Complete rough schedule for semester
    - Reevaluate deadlines and update as necessary
    - Ensure all tasks are assigned to a group member
- Sam
  - Continue testing and developing LLVM passes
- Maxwell
  - Begin work on the logic to handle the 8bit instructions
  - Test 8bit instructions
- Tristan
  - Begin presentation for PIRM 1